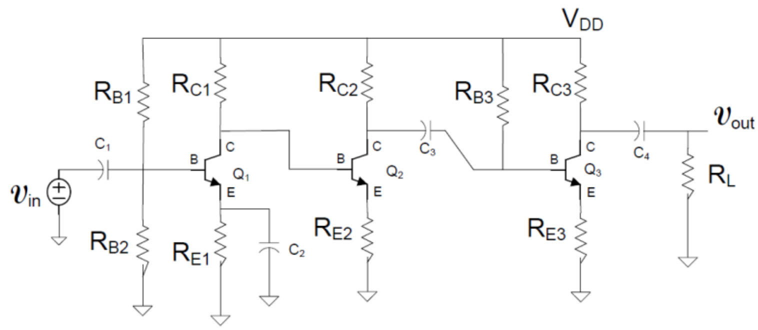
EE 330
Homework 10
Fall 2025
Due Friday, Oct 31 at noon.

Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX}$ = 250μA/V^2 and V_{Tn} = 0.4V, all p-channel transistors have model parameters $\mu_p C_{OX} = \mu_n C_{OX}/3$ and V_{Tp}= -0.4V. Correspondingly, assume all npn BJT transistors have model parameters J_S= 10^{-14}A/μ^2 and β=100 and all pnp BJT transistors have model parameters J_S= 10^{-14}A/μ^2 and β = 25. If the emitter area of a transistor is not given, assume it is 100μ^2 . Assume all diodes are characterized by the model parameters J_{SX}=0.5A/μm^2, V_{G0}=1.17V, and m=2.3.

Problem 1

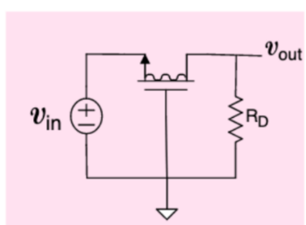
Draw the small signal equivalent circuit of the circuit shown below. Do not calculate the gain. Assume all capacitors are large.



Problem 2

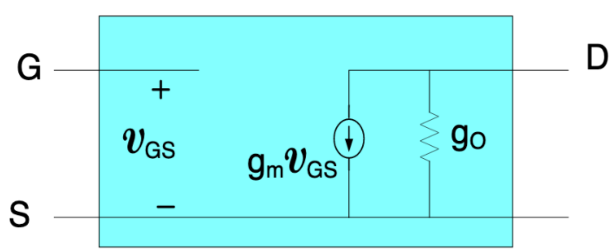
Assume the MOS transistor is operating in the saturation region and λ=0 for the circuit shown.

a) Find the small-signal voltage gain of the small-signal circuit shown in terms of the small-signal model parameters.
b) Find the small-signal voltage gain of this circuit in terms of the quiescent operating point of the transistor



Problem 3

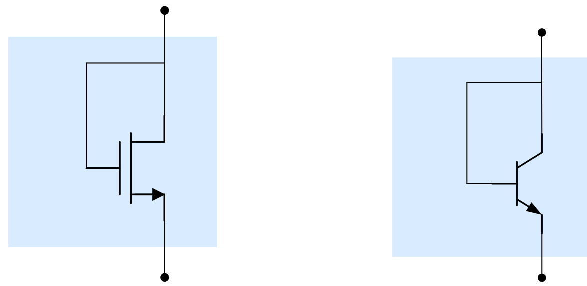
Recall from lecture that a saturated NMOS transistor can be modelled in the small-signal domain as follows:



where $g_m = \mu C_{ox}\frac{W}{L}(V_{GSQ} - V_T)$ and $g_o \approx \lambda I_{DQ}$. Derive the small-signal model of a PMOS device operating in the saturation region and compare with the model for the NMOS transistor.

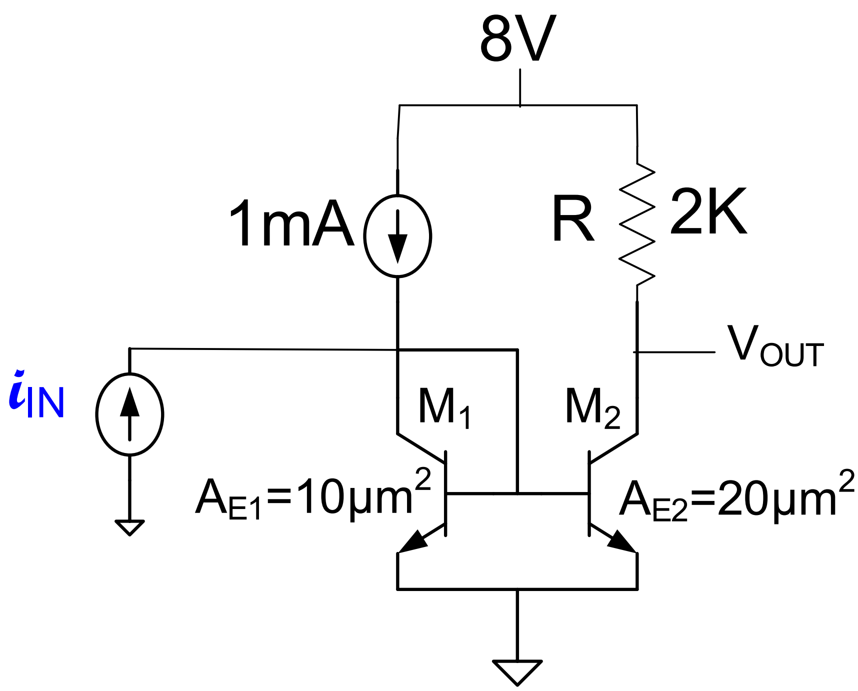
Problem 4* Consider the following circuits.

a) These circuits are both one-port devices. Obtain the small-signal model for the two devices.
b) Size the devices and determine the required quiescent current to force the small-signal impedance of devices to be 5KΩ.

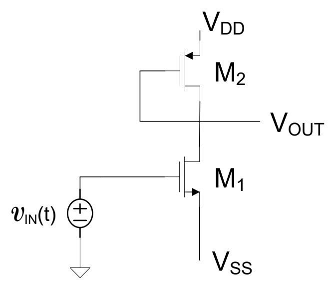


Problem 5*

a) Determine the quiescent current in the resistor R.
b) Determine the small-signal transresistance gain in terms of the small-signal model parameters. (the transresistance gain is the ratio of the small signal output voltage divided by the small signal input current).
c) Numerically obtain the small-signal transresistance gain of this amplifier.



Problem 6 Obtain an expression for the small signal output voltage in terms of the small signal parameters if the input is given by the expression $v_{IN}(t)=V_M\cos(\omega t+\theta)$. Assume M_1 is operating in the saturation region.

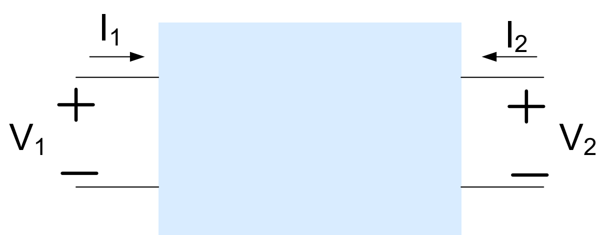


Problem 7 Design an amplifier using only MOS transistors, capacitors, and independent voltage sources that has a voltage gain of -10 when driving an external 10K resistor.

Problem 8 Consider a device characterized by the equations

$$I_1 = V_1 V_2^{\,2}$$

$$I_2 = 0.1e^{0.2V_1^2 V_2}$$



a. Determine the small signal model for a two-terminal device characterized by the equations given above

b. Determine the numerical values for the small signal model parameters if the quiescent value of the port voltages are V_2=1V, V_1=5V.

c. Determine the quiescent currents at the Q-point established in part b.

d. Determine the small signal currents i_1 and i_2 if the small signal voltages v_1 and v_2 were measured to be $1mV_{RMS}$ and $2mV_{RMS}$ respectively. Assume the same Q-point as established in part b.

Problems 9 and 10 Implement a positive edge triggered D flip-flop with asynchronous reset and active low enable pin using Verilog. When the flip-flop is disabled or reset, its output should be low. Design a testbench proving function using Verilog. Submit module code, testbench code, and Modelsim waveforms.